REMARKS

This paper is filed in response to the non–final Office Action mailed on July 25, 2006. Claims 1-10 and 14-17 are pending. Claims 1-10 and 14-17 have been examined and stand rejected. Applicants respectfully request reconsideration of Claims 1-10 and 14-17.

The Rejection of Claims 1-10 and 14-17 Under 35 U.S.C. § 112, Second Paragraph

Claims 1-10 and 14-17 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

In rejecting the claims, the Examiner states that the meaning and scope of the claims are indefinite and unclear referring to whether the "circuit patterns" formed in step (E) are the same circuit patterns that are formed in substep (c) of step (A).

The Manual of Patent Examining Procedure § 2173.02 states the guidelines for examination of the claims under this section. The Examiner's focus during examination of the claims for compliance with the requirement for definiteness of 35 U.S.C. § 112, second paragraph, is whether the claim meets the threshold requirements of clarity and precision, not whether more suitable language or modes of expression are available. In reviewing a claim for compliance with 35 U.S.C. § 112, second paragraph, the Examiner must consider the claim as a whole to determine whether the claim apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C. § 112, second paragraph, by providing clear warning to others as to what constitutes infringement of the patent. M.P.E.P. § 2173.02, p. 2100-211, Rev. 5, August 2006 (*citing Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1379, 55 U.S.P.Q.2d 1279, 1283 (Fed. Cir. 2000)).

Applicants submit the claims are not indefinite for the following reasons. Considering the whole claim, Step (E) of the claims recites forming circuit patterns on the outermost layers of

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a board obtained by pressing the circuit layers and the insulating layers, while in step (A)(c), the claims recite forming circuit patterns on the copper stack plate. Therefore, the circuit patterns of step (E) cannot be confused with the circuit patterns of step (A)(c), because the latter are formed on the copper stack plate and the former are formed on the outermost layers of a board obtained by pressing. Furthermore, in step (E), the phrase "circuit patterns" is not preceded by a definite article, such as "the"; therefore, it is clearly understood that the circuit patterns of step (E) do not refer to the circuit patterns in step (A)(c).

Therefore, the withdrawal of the rejection is respectfully requested.

The Rejection of Claims 16 and 17 Under 35 U.S.C. § 102(e)

Claims 16 and 17 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,826,830 (Egitto et al.).

For a reference to be anticipatory, the reference must exactly describe the claimed invention. Claim 16 recites "pressing the circuit layers and insulating layers and filling the via holes of the circuit layers with the conductive paste from the via holes of the insulating layers...." Webster's Ninth New Collegiate Dictionary, 1991, p. 462, states the meaning of "fill" is to "put into as much as can be held or conveniently contained" and "to supply with a full complement." Thus, using FIGURES 8 and 9 of the present specification to illustrate the meaning of the claims, the circuit layers 506a, b and c have via holes that are empty before pressing. Insulating layers 607a and b have conductive paste 606 aligned with the via holes in the circuit layers, before pressing. Next, referring to FIGURE 9, the conductive paste 606 fills the via holes of the circuit layers 506a, b and c during pressing.

In direct contrast, Egitto et al. describes that the conductive plugs 583 and 584 only serve to electrically couple the 2S1P substructures, and therefore, the conductive plugs 583 and 584 do not *fill* the via holes of the circuit layers as claimed. (See Col. 33, lines 8–21.)

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For a reference to be anticipatory, the reference must exactly describe the claimed invention. Because Egitto et al. does not exactly describe, at least, pressing the circuit layers and insulating layers and filling the via holes of the circuit layers with the conductive paste from the via holes of the insulating layers, the reference is not anticipatory. Furthermore, Egitto et al. does not teach or suggest the feature as well.

Accordingly, the withdrawal of the rejection of Claims 16 and 17 is respectfully requested.

The Rejection of Claims 1, 9, 14, and 15 Under 35 U.S.C. § 103(a)

Claims 1, 9, 14 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,826,830 (Egitto et al.) taken with U.S. Patent No. 5,258,094 (Furui et al.).

Claims 1 and 14 recite pressing the arranged circuit and insulating layers to fill via holes of circuit layers with a conductive paste of the insulating layers, while Claims 1, 14 and 15 recite forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers.

The Examiner states Egitto et al. teaches forming circuit patterns 567, 578, on the circuit layers before pressing (Figs. 24-25); whereas, Claims 1, 14, and 15 recite a step of forming circuit patterns on the outermost layers of a board obtained by pressing. However, the Examiner states Furui et al. teaches (at Figs. 14-18, Col. 5, line 38 through Col. 6) forming circuit patterns 68, 61, 21, 26, 66, 67 (Fig. 17) on the outmost layers of a board 1 obtained by pressing the circuit layers 14, 15, and the insulating layers 52 (Figs. 14-17). The Examiner concludes it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the multilayer printed circuit board of Egitto et al. by forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers, as taught by Furui et al. This is because of the desirability to form desired circuit patterns on the

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outermost layer of the board obtained by pressing the circuit layers and the insulating layers, wherein desired circuit patterns on the board can be subsequently formed and made for a particular circuit connection.

For a *prima facie* obviousness rejection, there must be either a suggestion or motivation either in the references or in the knowledge generally available to combine references, or to modify a reference, there must be a reasonable expectation of success, and all the claim limitations must be taught or suggested by the prior art.

The motivation is so vague as to be meaningless and simply begs the question. Egitto et al., as admitted by the Examiner, already forms the outermost circuit patterns before pressing; therefore, there is no motivation for forming the circuit patterns after pressing. Furthermore, in order to form such circuit patterns after pressing, the necessary conductive layers on the outermost surfaces of the board are not present in Egitto et al. Accordingly, any attempt to modify the invention of Egitto et al is bound to fail since Egitto et al. lacks teaching placing the necessary conductive layers on the outermost surfaces of the board with which to form any subsequent circuit layers. In the claimed invention, for example, the circuit layers 506b and 506c of FIGURE 8 have a copper plating layer 505 as the outermost layer which is used to form circuit patterns after pressing. Egitto et al. lacks teaching any such outermost layer. In fact, Egitto et al. forms the circuit patterns before pressing (Figure 24) and consequently does not leave copper material to further form circuit patterns after pressing.

Furthermore, Claims 1 and 14 have the added feature of pressing the arranged circuit and insulating layers to fill via holes of circuit layers with a conductive paste of the insulating layers. As discussed above, Egitto et al. fails to teach or suggest this aspect of claims, and Furui et al. does not cure this defect.

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Accordingly, the withdrawal of the rejection of Claims 1, 9, 14 and 15 is respectfully requested.

The Rejection of Claims 1, 3-5, 7-10, and 14-17 Under 35 U.S.C. § 103(a)

Claims 1, 3-5, 7-10, and 14-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0194303 (Kim et al.) taken with U.S. Patent No. 6,826,830 (Egitto et al.) and U.S. Patent No. 5,258,094 (Furui et al.).

Claims 1, 14 and 16 recite pressing the arranged circuit and insulating layers to fill via holes of circuit layers with a conductive paste of the insulating layers, while Claims 1, 14 and 15 recite forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers.

The Examiner admits that Kim et al. lacks teaching filling the via holes in the circuit layers with a conductive paste from the insulating layers. Therefore, the Examiner relies on Egitto et al. for purportedly teaching this aspect. However, in order to be able to fill the via holes of the circuit layers, the Examiner makes the assumption that Kim et al. alternatively teaches omitting the plugging of the via holes of the circuit layers with paste, and cites various passages including paragraphs 0061–0063 and 0055–0060 for this purported teaching, and further assumes that these circuit layers with the purportedly empty via holes would then be filled with paste during pressing.

Applicants submit that while the paragraphs cited by the Examiner may describe omitting paste from the via holes, such description does not mean that the via holes are left empty before pressing. At paragraph [0039], Kim et al. describes the problem with plugging via holes with paste. So therefore, in order to solve this problem, Kim et al. proposes to omit the paste and instead plate the via holes with copper. This is the explicit object of the invention of Kim et al. described at paragraph [0042]. Therefore, Kim et al. does not teach omitting the paste so that the

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via holes can be filled during pressing, but instead, Kim et al. teaches omitting the conductive paste and using plated copper in the via holes. This is also apparent from paragraph [0069] that explicitly teaches plugging the via holes 304 with plated copper, which in the immediately preceding paragraph [0068] are described to omit paste. Therefore, the purpose of omitting the paste from the via holes is to allow plating with copper, not for filling with paste during pressing. Applicants' position of the teaching of Kim et al. is further supported by reviewing Figure 7 that clearly shows that the via holes of the circuit layers 306a, b and c are filled with copper. Therefore, it is impossible to fill the via holes of the circuit layers with conductive paste from the insulating layers.

Furthermore, as discussed above, applicants' position is that Egitto et al. fails to teach or suggest pressing the arranged circuit and insulating layers to fill via holes of circuit layers with a conductive paste of the insulating layers, because Egitto et al. simply does not *fill* the via holes.

The Examiner further admits that Kim et al. fails to teach forming circuit patterns on the outermost layers of the board, and relies on the teaching of Furui et al.

As discussed above, the motivation or suggestion for forming circuit patterns on the outermost layers of the board, after pressing, when the reference to be modified has already formed them before pressing is so vague as to be meaningless, and simply begs the question.

Since a *prima facie* rejection requires both a suggestion or motivation, and that all the claim limitations be taught or suggested by the prior art references, and since there is no motivation or suggestion to combine Kim et al. with either Egitto et al. or Furui et al., and further because the combination of Kim et al. and Egitto et al. fails to teach all the claim limitations, the elements of a *prima facie* rejection have not been met.

Therefore, the withdrawal of the rejection of Claims 1, 3-5, 7-10, and 14-17 is respectfully requested.

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The Rejection of Claim 6 Under 35 U.S.C. § 103(a)

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0194303 (Kim et al.) taken with U.S. Patent No. 6,826,830 (Egitto et al.) and U.S. Patent No. 5,258,094 (Furui et al.), as applied to Claim 1 above and further in view of U.S. Patent No. 6,613,986 (Hirose).

Because Claim 6 is dependent from Claim 1, and Claim 1 has been shown to be neither anticipated or obvious in view of any one or a combination of references; accordingly, the withdrawal of the rejection of Claim 6 is respectfully requested.

CONCLUSION

In view of the foregoing amendment and remarks, applicants respectfully submit that Claims 1-10 and 14-17 are in condition for allowance. If the Examiner has any further questions or comments, the Examiner may contact the applicants' attorney at the number provided below.

Respectfully submitted,

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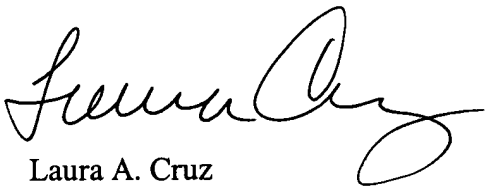

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